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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/879,335	06/11/2001	Vishnu K. Agarwal	MI22-1568	4063

21567 7590 04/01/2002

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EXAMINER
HUYNH, YENNHU B

ART UNIT	PAPER NUMBER
2813	+ 7

DATE MAILED: 04/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/879,335	AGARWAL ET AL.	
	Examiner	Art Unit	
	Yennhu B. Huynh	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claims 51-57 have been cancelled by Amendment filed on1/11/02.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Capacitor Forming Methods.

Claim Objections

Claim 43 objected to because of the following informalities: line 10, the limitation --the dielectric layer-- should be changed to read as --the high K capacitor dielectric layer--. Appropriate correction is required.

Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (U.S. 5,783,462) in view of Gonzalez (U.S. 6,300,188B1).

Huang at figs. 1-5 in related art col. 1-6 disclose a stacked capatitor DRAM cell, which including the steps of forming an insulation layer 14 over a substrate including an electronic device comprise transistor 16; a barrier layer over the substrate; an opening at least into the insulation layer 14 (fig. 3-5); a capacitor dielectric 25 layer at least within the opening; a congruent opening through the barrier layer; where in the opening is formed completely through the insulation layer; forming a lower capacitor electrode 24A/24B before forming the dielectric layer. Huang also disclose an second insulation 28 layer over the barrier layer; an opening 66 into the second insulation layer; a capacitor dielectric layer 25 over the barrier layer.

However, Huang do not disclose a barrier layer to threshold voltage inducing material into the electronic device and a high K capacitor dielectric.

Gonzalez in related art col. 1-10 disclose a barrier layer 41 for restricting the conductivity enhancing impurity into contact region 28 & 29 through migration , reaches to the electronic device comprising transistor 18 to degrade the sub threshold voltage of the access transistor. (col. 6, lines 38-43); and a high capacitor dielectric constant 46 (col. 7, lines 7,8).

It would have been obvious to one having skill in the art at the time the invention was made to combine the teachings from Gonzalez 's process in forming a barrier layer retarding movement of the voltage inducing material into the electronic device comprising transistor to degrade the sub threshold voltage of the access transistor, and a high K capacitor dielectric, into Huang 's process. This modification would complete a method of forming capacitor as the claimed invention.

Claims 36-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prall et al. (5,866,453) in view of Gonzalez (U.S. 6,300,188B1).

Prall et at figs. 1-18 in related art col. 1-10 disclose an aligning capacitor structure, which include the steps of forming an insulation layer 36 over a substrate 12 including an electronic device 22; an opening 38 into the insulation layer, the opening having a sidewall 34 (fig. 2); a capacitor electrode 40 at least within the opening and over the sidewall (fig. 3,4); a silicon nitride barrier layer 43 over the structure formed (co. 6, lines 26-28); a capacitor dielectric 44 over the structure previously formed (col. 6, line 53-54).

However, Prall et al. do not disclose a barrier layer to threshold voltage inducing material into the electronic device.

Gonzalez in related art col. 1-10 disclose a barrier layer 41 for restricting the conductivity enhancing impurity into contact region 28 & 29 through migration , reaches to the electronic device comprising transistor 18 to degrade the sub threshold voltage of the access transistor. (col. 6, lines 38-43); and a high capacitor dielectric constant 46 (col. 7, lines 7,8).

It would have been obvious to one having skill in the art at the time the invention was made to combine the teachings from Gonzalez 's process in forming a barrier layer retarding movement of the voltage inducing material into the electronic device comprising transistor to degrade the sub threshold voltage of the access transistor, ,

into Prall et al. 's process. This modification would complete a method of forming capacitor as the claimed invention.

Cited Prior Art

Thakur et al. (U.S. 6,251,720 B1) in related art disclose a high dielectric constant capacitive dielectric film. The process include a Ta2O5 capacitor dielectric layer; a barrier layer of silicon nitride formed over the capacitor electrode and under the dielectric; an electronic device in the substrate; a N2O ambient for inducing material; an annealing the dielectric comprises with oxide. However, Thakur do not disclose a barrier layer to threshold voltage into the electronic device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yennhu B. Huynh whose telephone number is 703-308-6110. The examiner can normally be reached on M-F 8.30AM-7.00PM.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

YNBH,

3/20/02

K Christiansen

Keith Christiansen
Primary Examiner
Technology Center 2800